What is claimed is:

1. A shift register having a plurality of stages each providing a gate line driving signal to a corresponding gate line of a display panel, the stages each comprising:

a pull-up part to generate a current gate line driving signal having a first state in response to a first control signal and a clock signal;

a pull-down part to generate the current gate line driving signal having a second state in response to a second control signal;

a pull-up driver to generate the first control signal to control the pull-up part in response to an adjacent previous gate line driving signal provided from an adjacent previous stage, an adjacent following gate line driving signal provided from an adjacent following stage, and an input voltage signal externally provided; and

a pull-down driver to generate the second control signal to control the pull-down part in response to the first control signal and the input voltage signal,

wherein the second control signal swings between first and second voltage levels in association with the input voltage signal that swings between predetermined voltage levels.

2. The shift register of claim 1, wherein the second control signal is a pulse signal having a period substantially equal to a period of the clock signal.

3. The shift register of claim 1, wherein the second control signal is a pulse signal having a period substantially equal to a half of a period of the clock signal.

4. The shift register of claim 1, wherein the second control signal is a pulse signal having rising edges each of which is synchronized with a transition of the clock signal.

5. The shift register of claim 1, wherein the second control signal is a pulse signal having rising edges each of which is synchronized with a rising edge of the clock signal.

6. The shift register of claim 1, wherein the second control signal is a pulse signal having a phase leading a phase of the clock such that every rising edge of the second control signal leads every transition of the clock signal by a selected time period.

7. The shift register of claim 1, wherein the second control signal is a pulse signal having a phase leading a phase of the clock such that every rising edge of the second control signal leads every rising edge of the clock signal by a selected time period.

8. The shift register of claim 1, wherein the pull-up part includes a pull-up transistor having a conduction path between a terminal receiving the clock signal and a terminal generating the current gate line driving signal, and a gate electrode receiving the first control signal from the pull-up driver; and the pull-up driver includes a hold transistor to maintain a voltage level at the gate electrode of the pull-up transistor at a selected voltage level, the hold transistor having a gate electrode receiving the second control signal from the pull-down driver.

9. The shift register of claim 8, wherein an amplitude of a gate-source voltage of the hold transistor is larger than two times a threshold voltage of the hold transistor.

10. The shift register of claim 8, wherein the input voltage signal has an amplitude larger than seven times a threshold voltage of the hold transistor.

11. The shift register of claim 1, wherein the pull-down part includes a pull-down transistor having a conduction path between a terminal generating the current gate line driving signal and a terminal having a selected voltage level, and a gate electrode receiving the second control signal from the pull-down driver.

12. The shift register of claim 11, wherein an amplitude of a gate-source voltage of the pull-up transistor is larger than two times a threshold voltage of the pull-up transistor.

13. The shift register of claim 11, wherein the input voltage signal has an amplitude larger than seven times a threshold voltage of the pull-up transistor.

14. The shift register of claim 1, wherein the pull-down driver includes:

an inverter to generate a fourth control signal in response to the input voltage signal and the third control signal from the pull-up driver; and

a deterioration compensation part to generate the second control signal in response to the input voltage signal, the third control signal from the pull-up driver, and the fourth control signal from the inverter.

15. The shift register of claim 14, wherein the inverter includes:

a first transistor having a conduction path between a terminal receiving the input voltage signal and a first node, the first transistor operating as a diode; and

a second transistor having a conduction path between the first node and a terminal having a selected voltage level and a gate electrode receiving the third control signal from the pull-up driver,

wherein the inverter generates the fourth control signal from the first node.

16. The shift register of claim 15, wherein the deterioration compensation part includes:

a third transistor having a conduction path between the terminal receiving the input voltage signal and a second node and a gate electrode receiving the fourth control signal from the inverter; and

a fourth transistor having a conduction path between the second node and the terminal having the selected voltage level and a gate electrode receiving the third control signal from the pull-up driver,

wherein the deterioration compensation part generates the second control signal from the second node.

17. The shift register of claim 16, wherein the second control signal is provided to a gate electrode of a pull-down transistor in the pull-down part and a gate electrode of a hold transistor in the pull-up driver, the input voltage signal having an amplitude larger than seven times a threshold voltage of the pull-down transistor or the hold transistor.

18. A method of driving a transistor having gate, drain and source electrodes, the method comprising:

applying a first voltage signal to the drain electrode;

applying a second voltage signal to the source electrode; and

applying a third voltage signal to the gate electrode to control an electrical conduction path between the drain and source electrodes,

wherein the third voltage signal swings between predetermined voltage levels, so that a gate-source voltage signal established between the gate and source electrodes of the transistor swings between first and second voltage levels at a selected period.

19. The method of claim 18, wherein the gate-source voltage signal has an amplitude larger than two times a normal threshold voltage of the transistor.